OpenHPSDR on an Altera SoC

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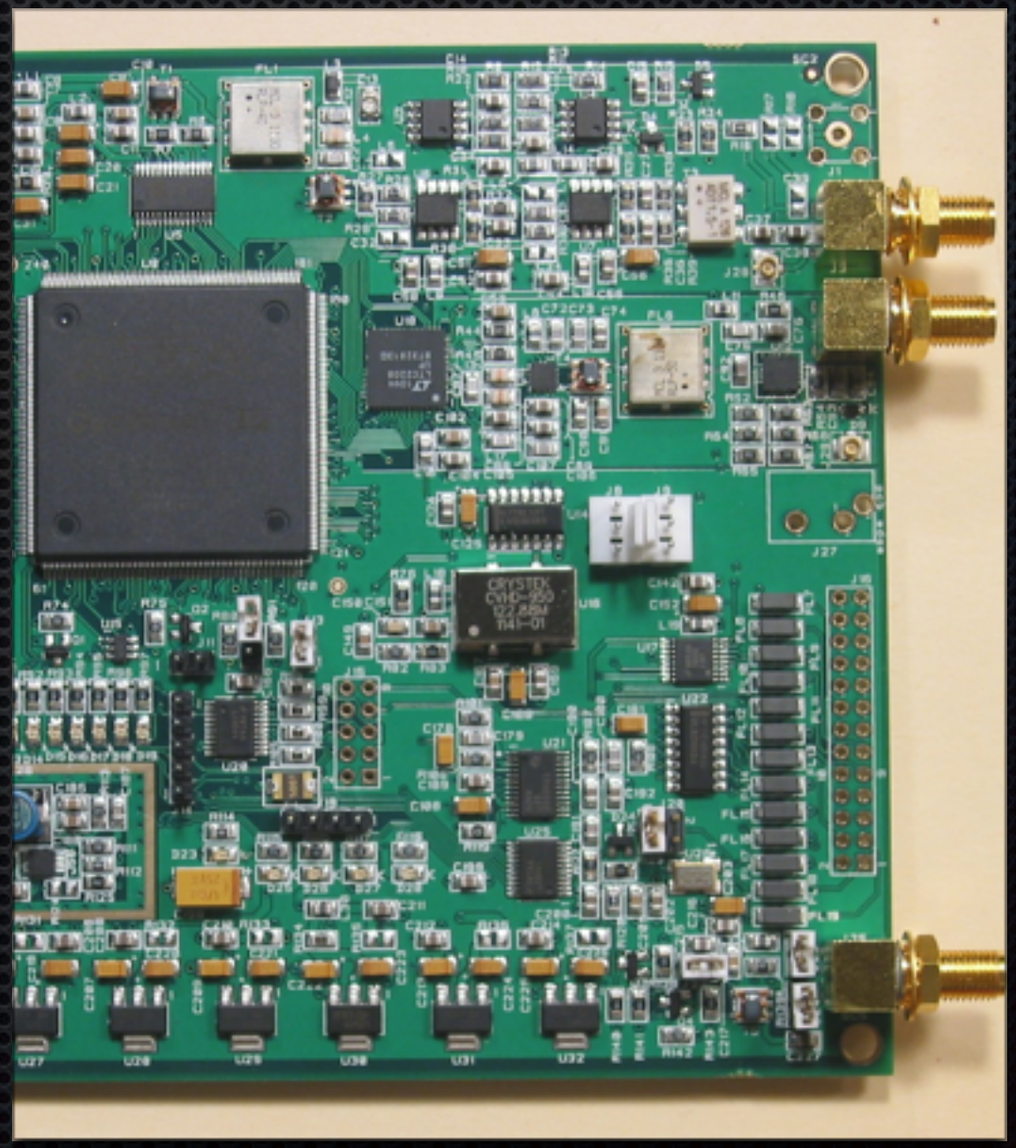
About the Author

- Licensed in 1986 as KB7AKH
- Programming since Age 5
- Spent 15 years in Systems and Network Administration
- Volunteer Counsel for Oregon
- Vice President, TAPR

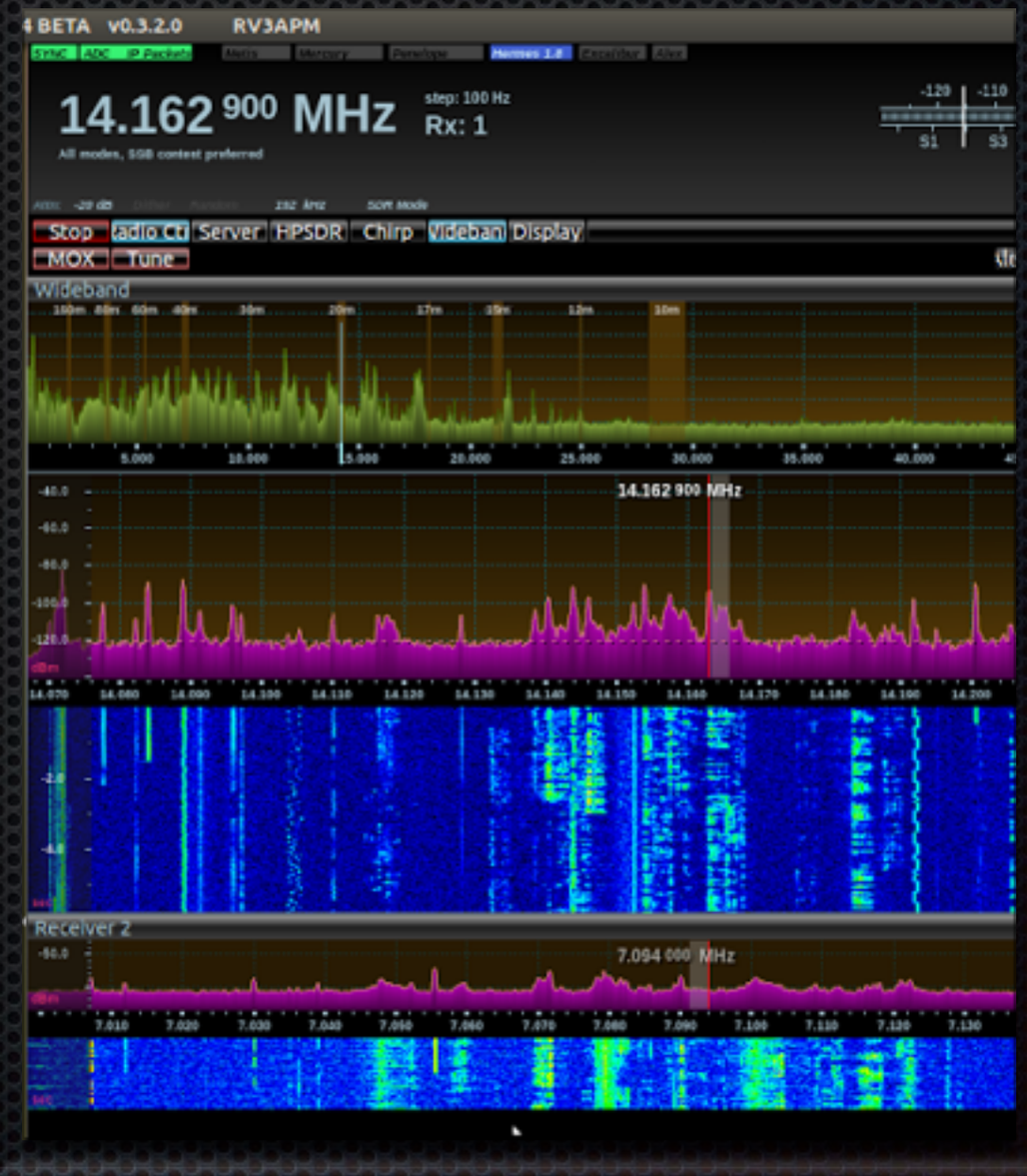
Current Generation OpenHPSDR

- Altera Cyclone FPGA based
- Firmware entirely written in Verilog
- Basic UDP/IP networking stack
- Firmware update via specialized protocol over Ethernet



Problems with Current System

- TCP/IP stack is really stupid
- Updating firmware can be difficult
- Changing firmware protocols can be time consuming and problematic
- Firmware development relegated to those that know Verilog

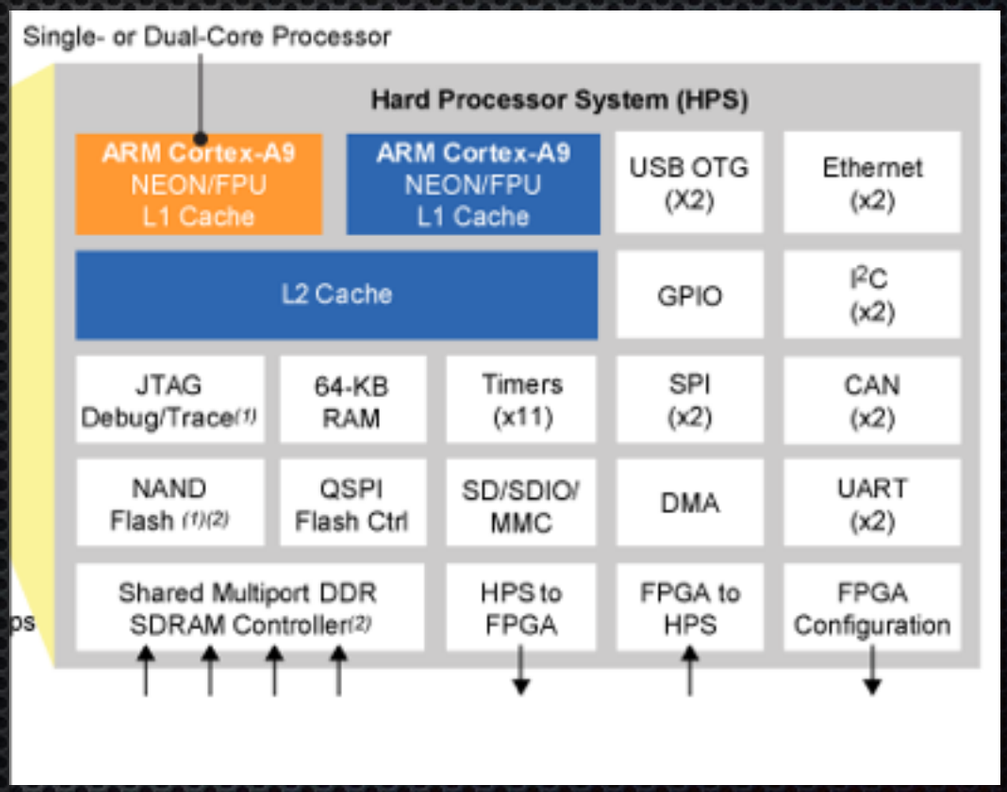


Altera Cyclone V System on a Chip (SoC)

- Cyclone V FPGA
  - Logic Elements
  - Hard Memory Controller
  - Hard LVDS Transceivers

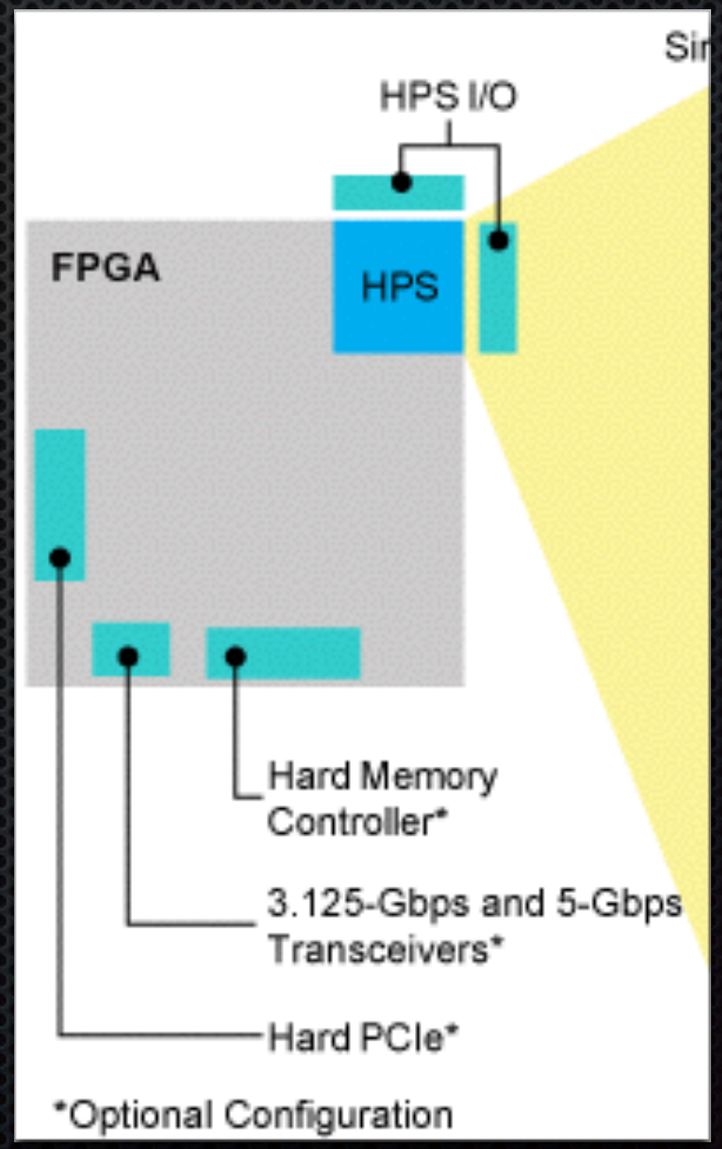
Altera Cyclone V System on a Chip (SoC)

- Hard Processor System (HPS)
  - Dual Core ARM Cortex A9 Up to 925MHz
  - SD Card Controller
  - Dual Gigabit Ethernet MACs
  - Dual USB-OTG Controllers



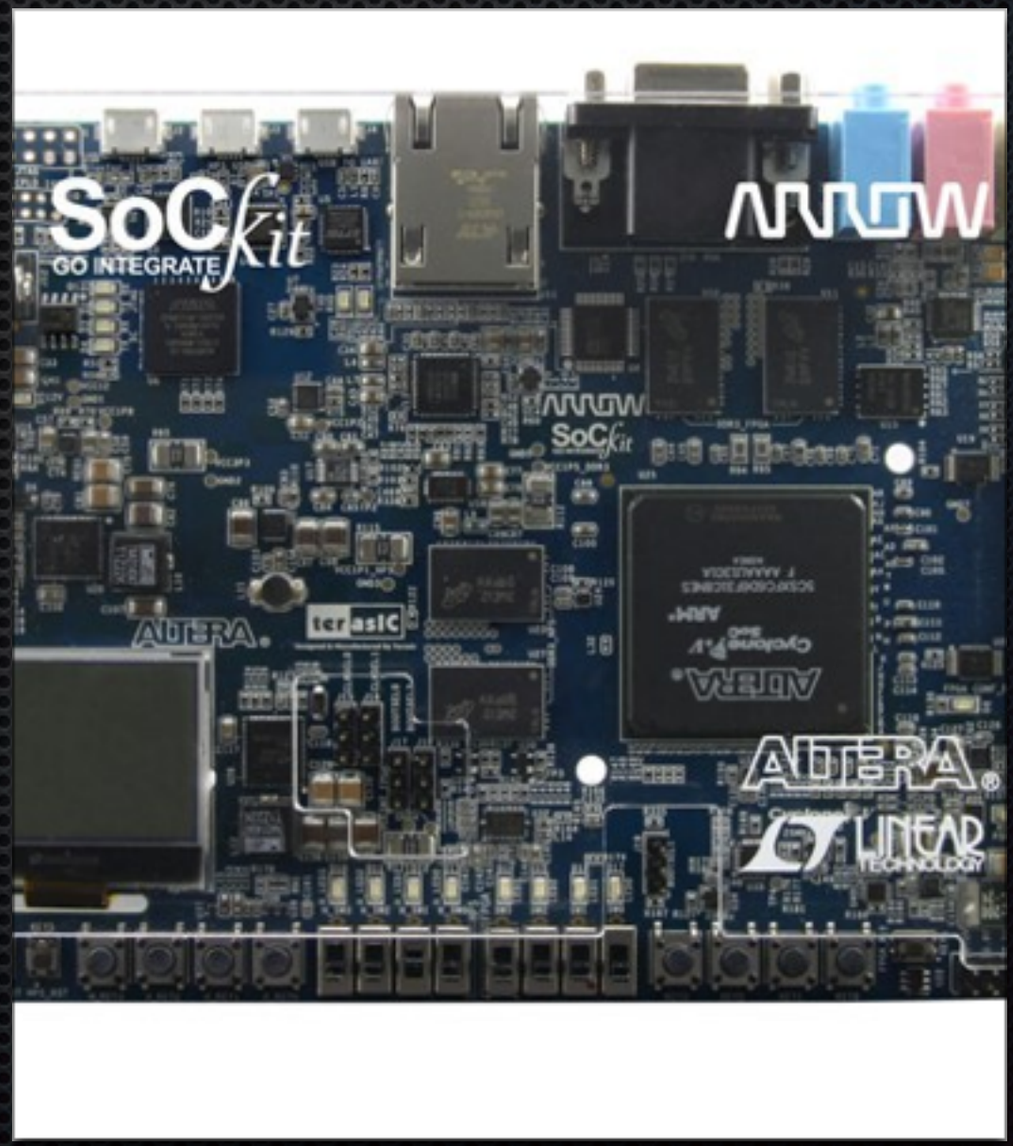
Altera Cyclone V System on a Chip (SoC)

- FPGA Bridges
  - 32, 64 or 128 bits Wide
  - FPGA to HPS
  - HPS to FPGA
  - Lightweight HPS to FPGA
  - Capable of over 100 Gbps peak throughput



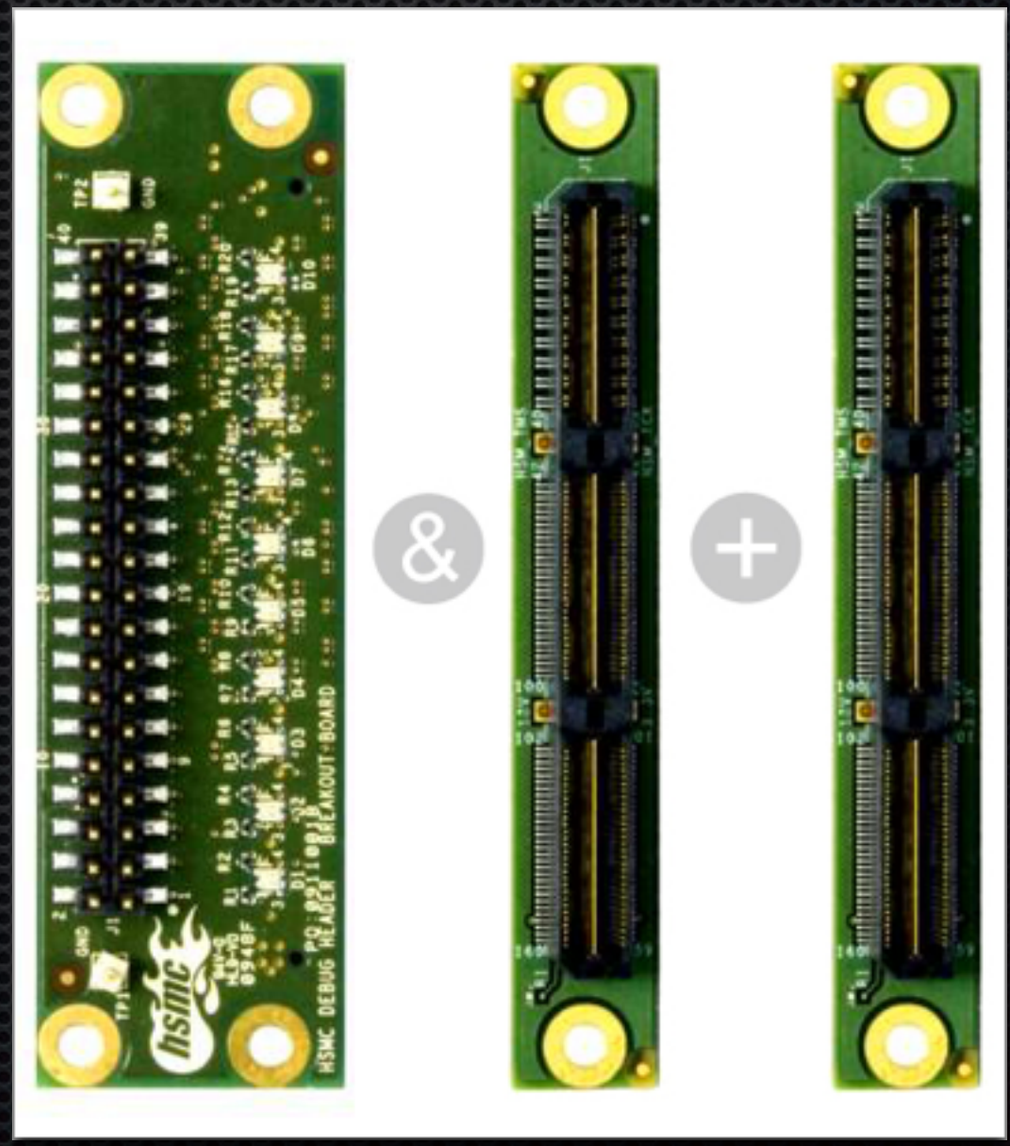
Terasic/Arrow SoCKit

- Altera 5CSXFC6D6F31C8NES
  - 600MHz Dual Core
  - 115,000 Logic Elements
- 1 x 10/100/1000 Port
- 1Gb Memory each for FPGA and HPS
- Built in USB Blaster
- Built in USB UART
- USB OTG Port
- MicroSD Card
- $299 from Arrow Electronics



High Speed Mezzanine Connector (HSMC)

- Multi-Gigabit Connection Standard
- Provides JTAG, Power, Clock, High Speed Serial and Single Ended/ Differential I/O
- Can Connect FPGA to External Device Cards

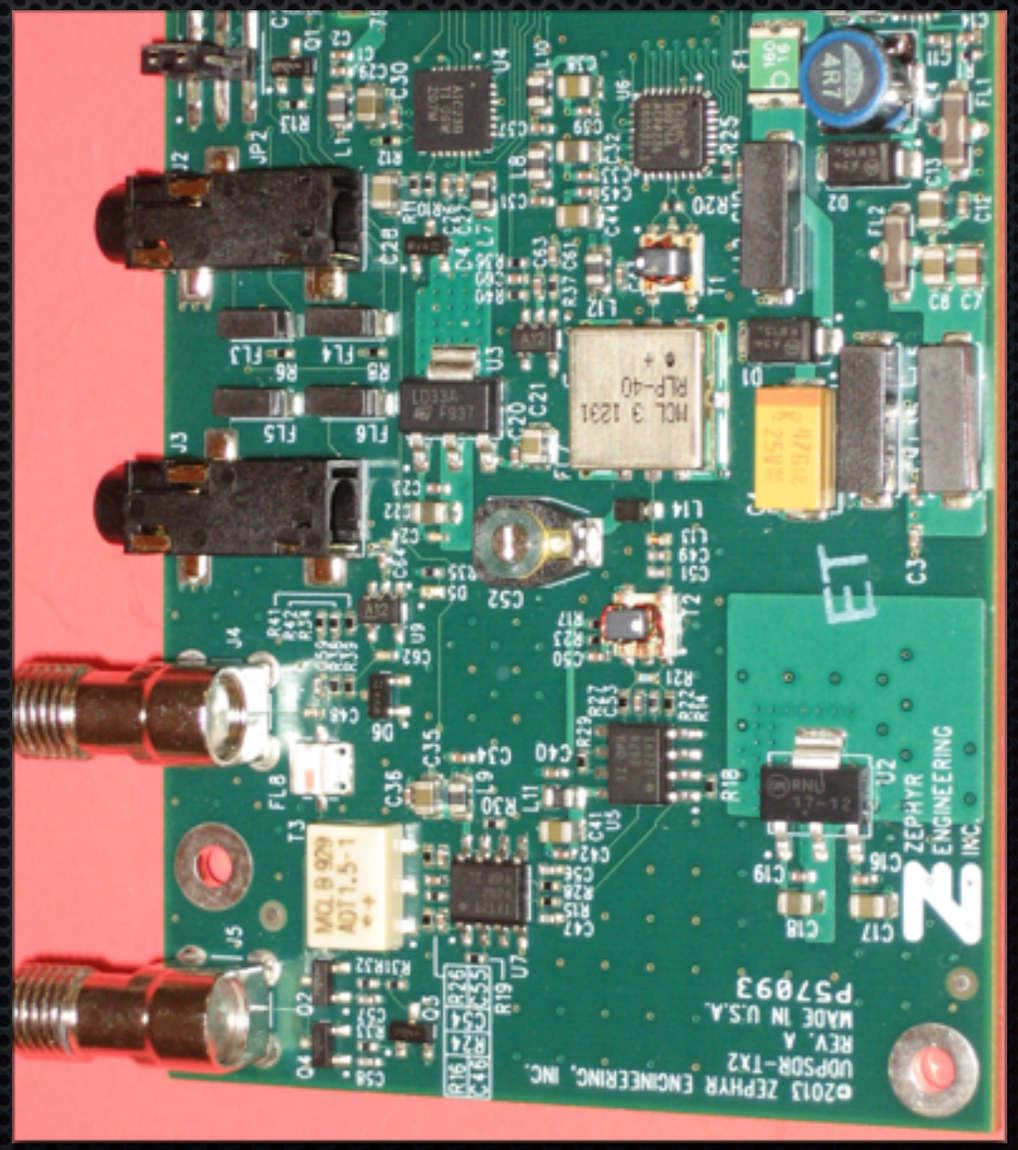


iQuadLabs UDPSDR-HF2

- LTC2208 from OpenHPSDR Mercury and Hermes
- $399 at www.iquadlabs.com

iQuadLabs UDPSDR-TX2

- Same DAC as HSPDR Hermes/Penelope/ PennyLane
- $179 from www.iquadlabs.com

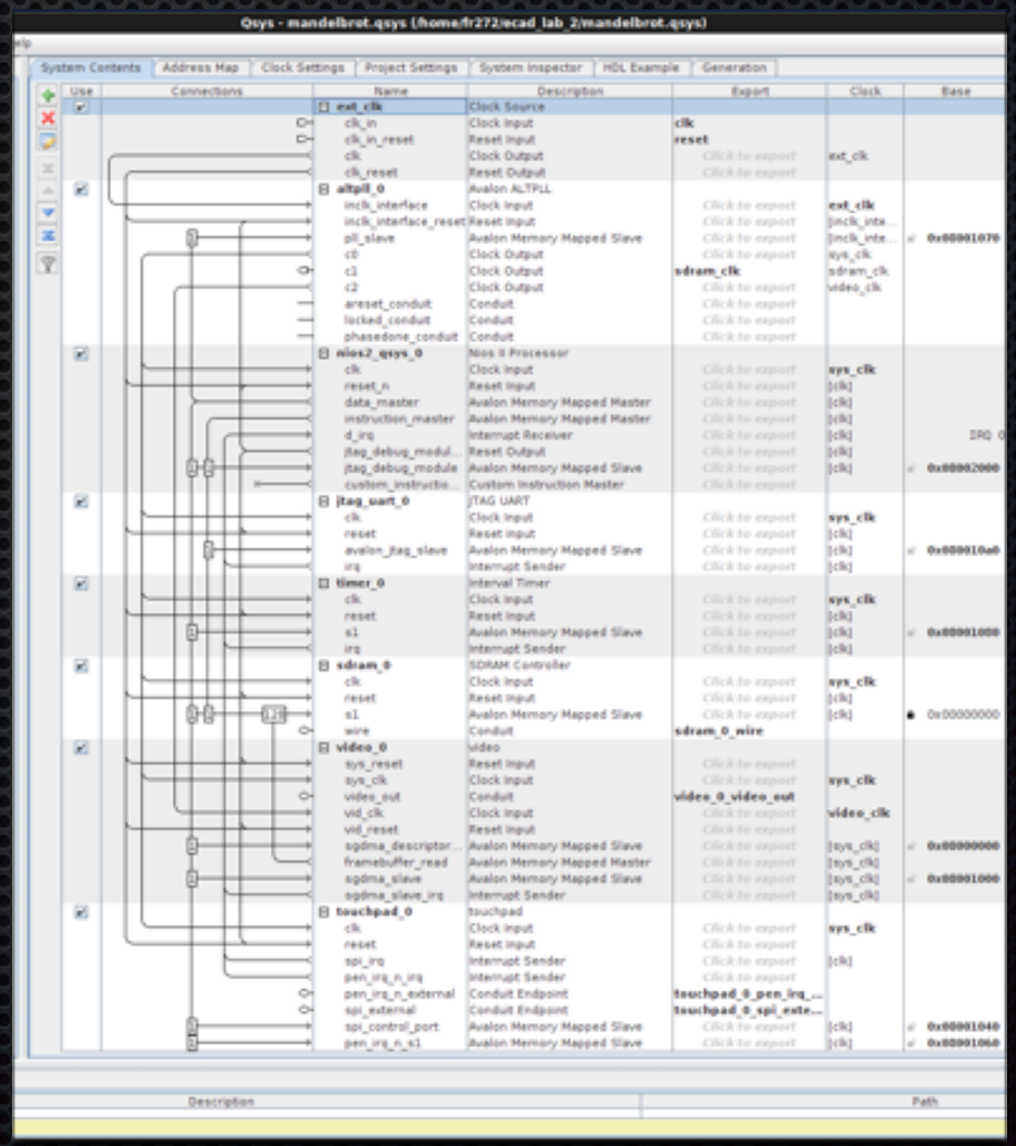


iQuadLabs HSMC Board

- Takes a UDPSDR-HF2 and UDPSDR-TX2 and interfaces them to a SoCKit over the HSMC connector
- Coming Soon and Pricing TBA

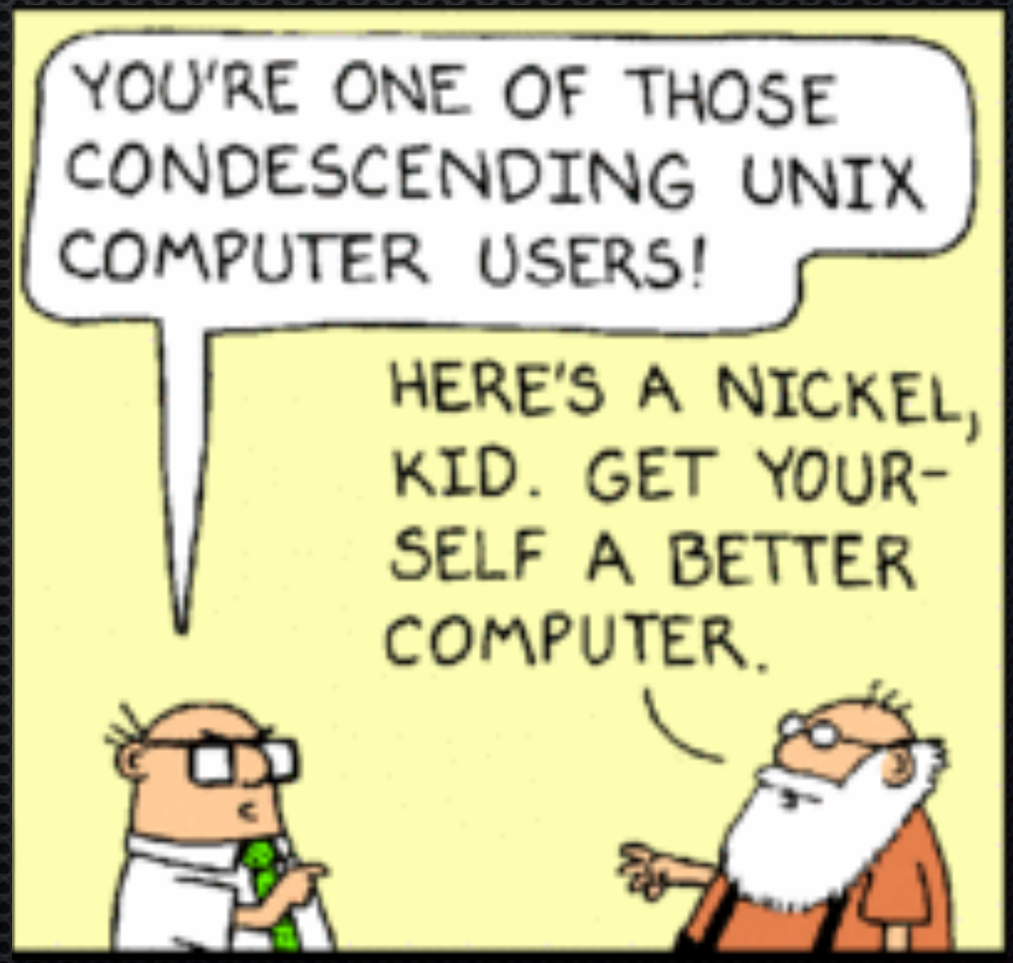
Altera Qsys

- Point and Click Verilog Generation
- Uses Components with Standard Interfaces (Avalon)
- Developers Can Write Custom Avalon Interface Components in Verilog
- Wire Together HPS Interrupts and Signals into FPGA Components



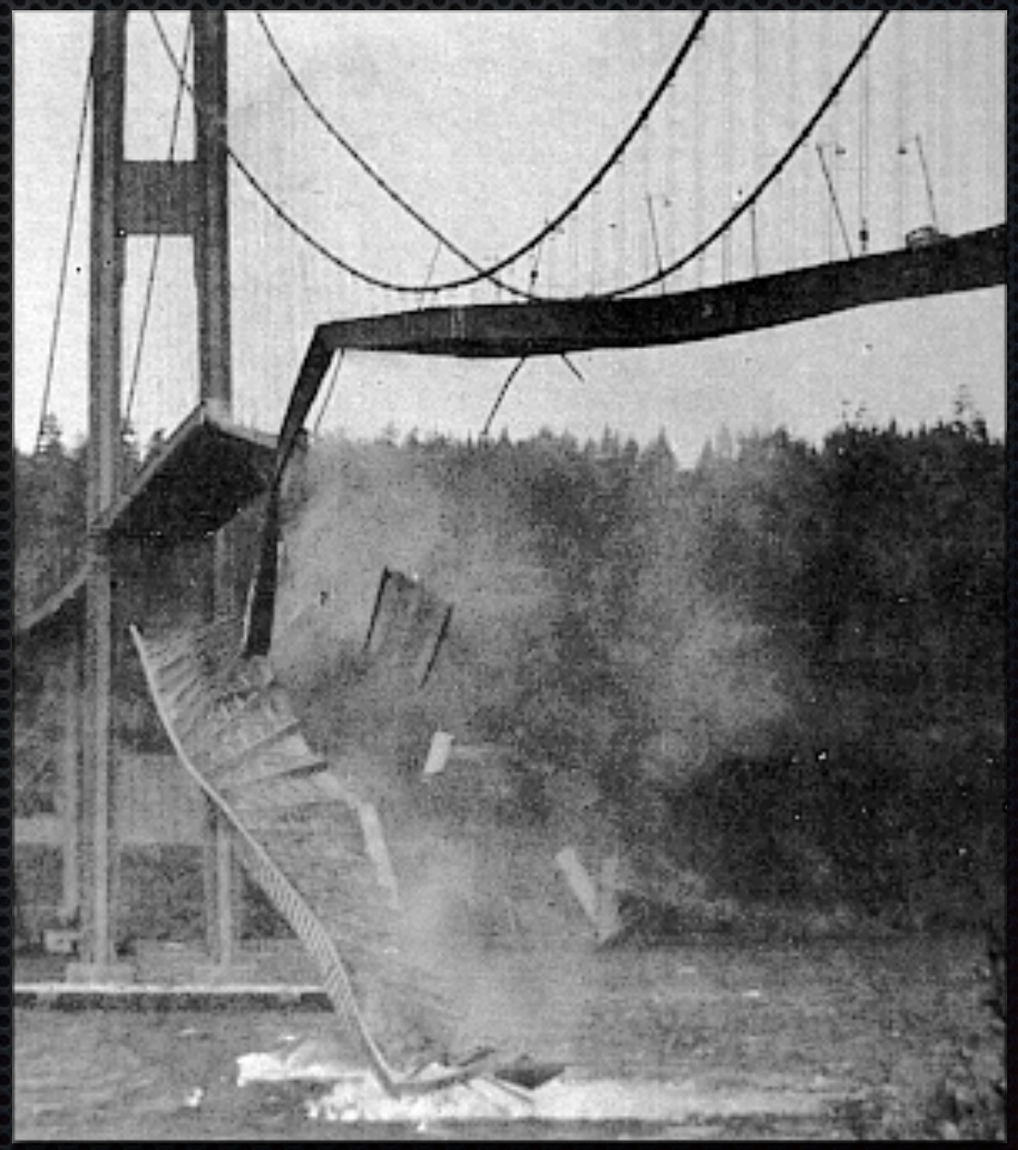
HPS System Software

- It Can Run Linux
  - Sorry No Windows
- Uses the Yocto Project to Create a Custom Embedded Distro
  - www.yoctoproject.org
- Can Boot from Either SD Card or Onboard Flash Chips
- Uses the U-Boot Bootloader
  - Needs a “Preloader” to Set Up Pins
- www.rocketboards.org is a community website for Linux on Altera SoC



FPGA Bridge System Interface

- Each Bridge Mapped as Registers into Memory
- 1Gb Address Space
- 64 Interrupts from the FPGA
- Qsys Components Available to Allow FPGA Direct Access to HPS SDRAM and HPS Direct Access to FPGA SRAM or DRAM
- FPGA Manager Allows Programming FPGA from Linux
  - dd if=image.rbf of=/dev/fpga0 bs=1M



Potential OpenHPSDR SoC System

- FPGA Still Does Initial Filtering and Decimation into Firmware Receivers
- Each Firmware Receiver Presented to Userland as /dev/hpsdrrx[0-9]+
- Transmitter Presented as /dev/hpsdrtx0
- Control of Frequency, etc. in Linux /sys Filesystem
- Userland Can Take Samples from Device Files and Talk Whatever Protocol Necessary
- Web Based Systems Management Interface

Advantages of Architecture

- Flexibility in Protocol Implementation
  - Easier in Linux
  - Uses Linux TCP/IP Stack
  - Can Speak Multiple Protocols Simultaneously
  - Potential Integration of GNU Radio
  - Web Management is Easier, More Powerful and Inherently Cross-Platform

Project Sisyphus Proposal

- New HPSDR Board
- Can Use Existing HPSDR Boards
- Has HSMC Connectors for “Second Generation” HPSDR Boards
- Altera SoC is Embedded on Backplane
  - No Metis or Ozy equivalent

Questions?

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