DOWNTHE RABBITHOLE

A Software Guy's Adventure in Hardware Land



ABOUTTHE AUTHOR

- I'm down with O.P.P.
- Still a lawyer



Thanks to Jakob McDermond for the lawyer joke.

PROJECT REFRESHER

Arrow SoCKit board with an Altera Cyclone V SoC

- SDRStick HF2/AD1/TX1
- Move much of the FPGA code to Linux
- Appropriate kernel/ userspace separation



FPGA ARCHITECTURE

- CORDIC implements mixer
- CIC provides initial decimation
- FIR provides final decimation and shape correction



DECIMATION

- Reduces data rate to ease processing data
 - ADC produces 1.966 Gbit/sec of data
- Shannon's sampling theorem says we need 2x bandwidth (Nyquist Frequency)
- I and Q double the effective sample rate
- Merely decimating creates aliases, we need to filter too



FPGA RESOURCES

A given FPGA only has a certain number of "Logic Elements"

- There are also limits on the number of:
 - SRAM Memories
 - Multipliers



WHY CIC?

- "Cascaded Integrate and Comb" Filter
- Single pole decimator
- Uses only addition and subtraction
- Transition band is wide and not very flat





COMPENSATING FIR

- Compensates for CIC shape
- Narrow transition band
- Low decimation factor
- Uses one multiply per tap





KERNEL DRIVER

Hardware FIFO sends IRQ at configurable level

- Interrupt controller reads from Hardware FIFO into kernel FIFO
- read(2) reads out of the kernel FIFO

	in	
Kf;fc	L	
	XII	
1	5	
	dota	here
out		

USERLAND DAEMON

- Reads from /dev/hpsdrrx0
- Manipulates controls in /sys
- Deals with all network traffic
- Multithreaded



HIERARCHY OF PAIN AND SUFFERING

Poison Oak Vserland Software

Root Canal

Kernel Driver

Amputation Without Anesthetic

FPGA Firmware



- Userland: GDB, printf, etc.
- Kernel: KDB, kprintf, etc.
- FPGA: LEDs, SignalTap

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0x80483b2 (main+14): add eax 0xf
0x80483b5 cmain+17>: add cax.0xf
Av8483b8 (main+20): the eav 8v4
By8B483bb (main+23): shl eax, By4
8x88483be (main+26): sub esp.eax
0x80483c0 (main+28): mov eax.ds:0x80484f4
0x80483c5 <main+33>: mov DWORD PTR [ebp-24].eax</main+33>
0x80483c8 <main+36>: mov al.ds:0x80484f8</main+36>
0x80483cd (main+41): mov BYTE PTR [ebp-20].al
0x80483d0 <main+44>: sub esp.0xc</main+44>
0x80483d3 <main+47>: push 0x80484f9</main+47>
0x80483d8 <main+52>: call 0x80482b8 <printf@plt></printf@plt></main+52>
0x80483dd <main+57>: add esp.0x10</main+57>
0x80483e0 <main+60>: leave</main+60>
Breakpoint 1, 0x080483aa in main ()

VERILOG

Vendors only implement what they want

- Have to remember you're creating hardware
- Not all language constructs can be in hardware
- Testbench vs. Implementation





BUILDTIME

Userland

republic:openhpsdrd mcdermj\$ time make

real	0m0.132s
user	0m0.088s
sys	0m0.034s

Kernel Module

republic:hpsdr mcdermj\$ time make default

real 0m1.046s user 0m0.662s sys 0m0.301s

FPGA

mcdermj@commune:~/sdrstick\$ time make
real 12m8.360s
user 14m27.640s
sys 0m31.328s

MODELSIM

Useful for checking syntax before your 12 minute compile

- Unfortunately supports more of the standard than Quartus
- Just debugger enough to be annoying

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MATLAB

- Great for filter design
- Yet Another Language
- Seems to not tell the whole story sometimes



QUESTIONS?



Software Developer



FPGA Developers (In Natural Habitat)