DOWN THE ~~RABBIT HOLE~~ RATHOLE

A Software Guy's Adventure in Hardware Land

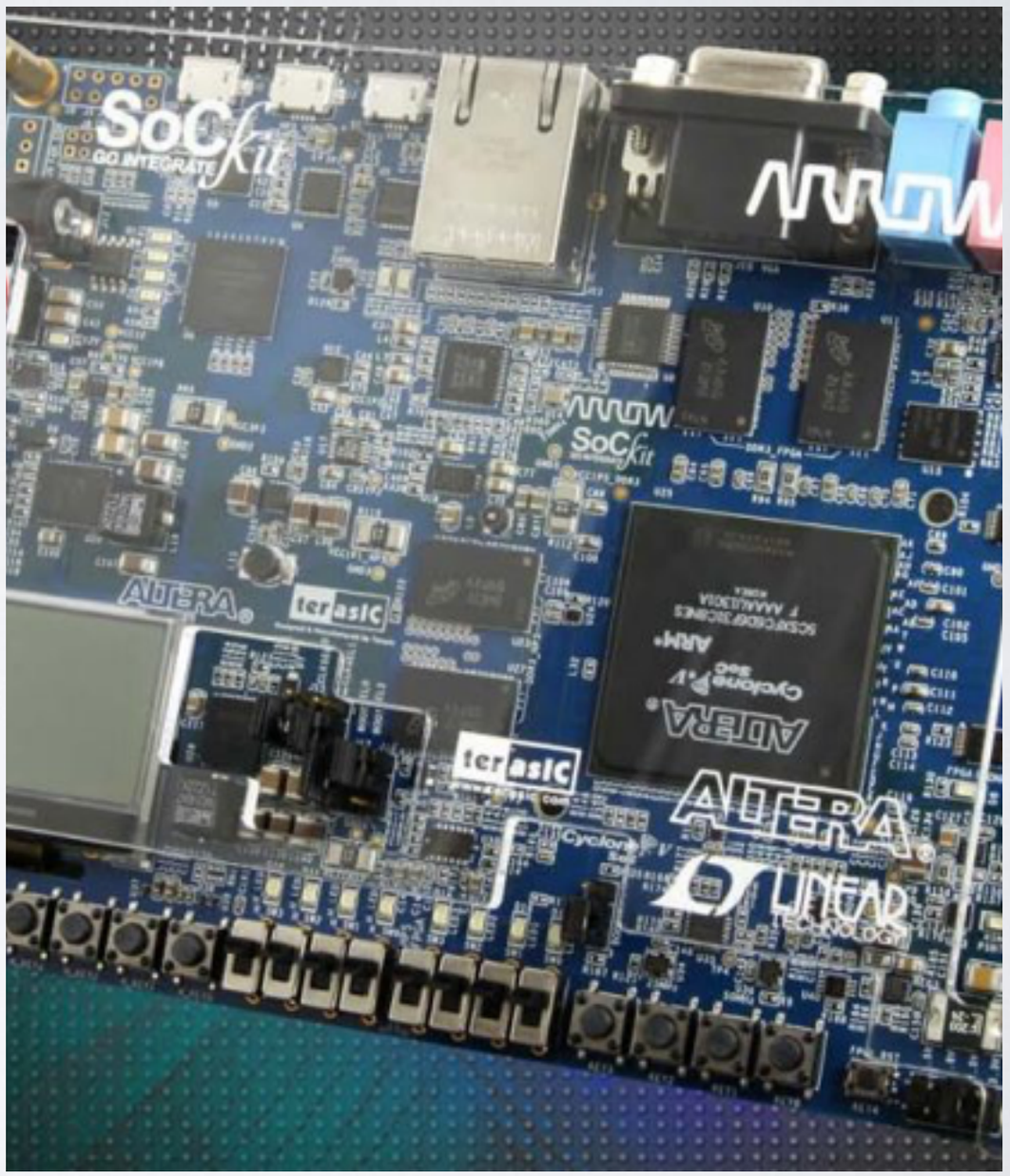
ABOUT THE AUTHOR

- I'm down with O.P.P.
- Still a lawyer

Thanks to Jakob McDermond for the lawyer joke.

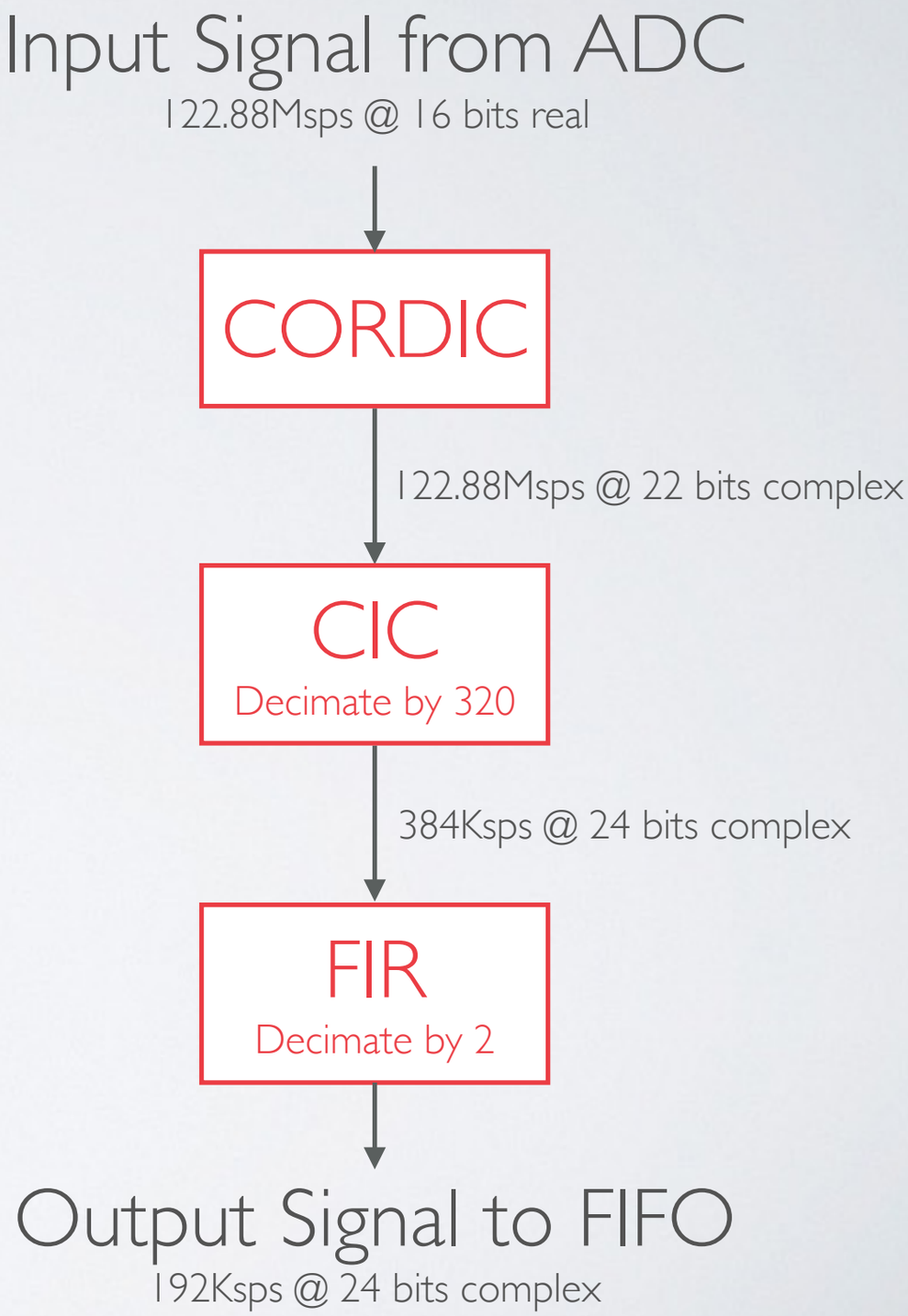
PROJECT REFRESHER

- Arrow SoCKit board with an Altera Cyclone V SoC
- SDRStick HF2/AD1/TX1
- Move much of the FPGA code to Linux
- Appropriate kernel/ userspace separation



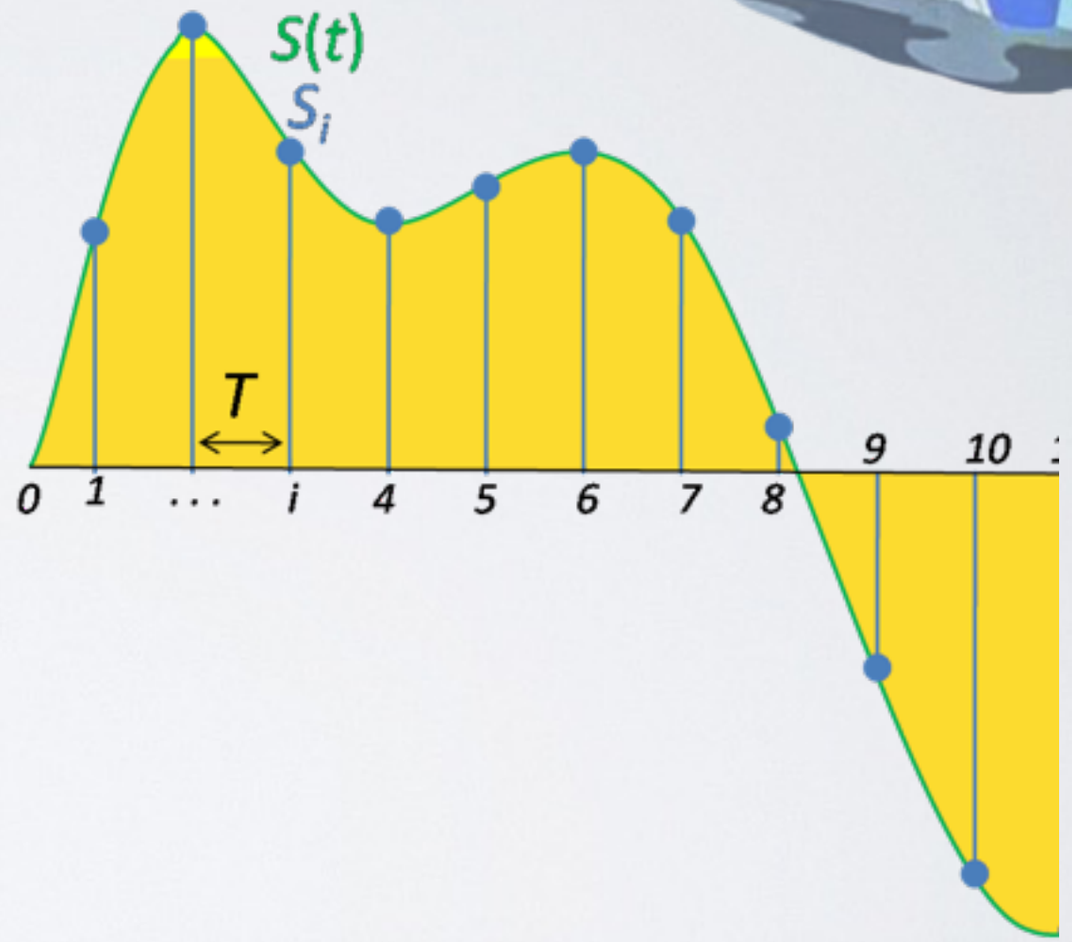
FPGA ARCHITECTURE

- CORDIC implements mixer
- CIC provides initial decimation
- FIR provides final decimation and shape correction



DECIMATION

- Reduces data rate to ease processing data
  - ADC produces 1.966 Gbit/sec of data
- Shannon's sampling theorem says we need 2x bandwidth (Nyquist Frequency)
- I and Q double the effective sample rate
- Merely decimating creates aliases, we need to filter too

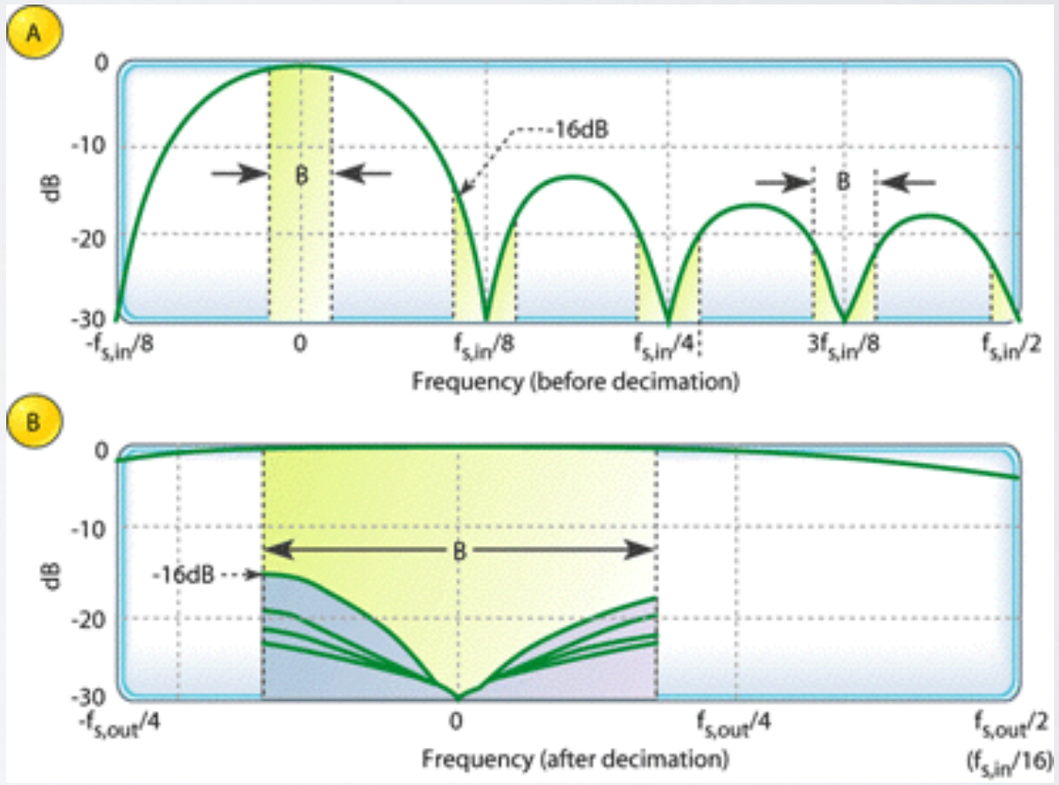


FPGA RESOURCES

- A given FPGA only has a certain number of "Logic Elements"
- There are also limits on the number of:
  - SRAM Memories
  - Multipliers

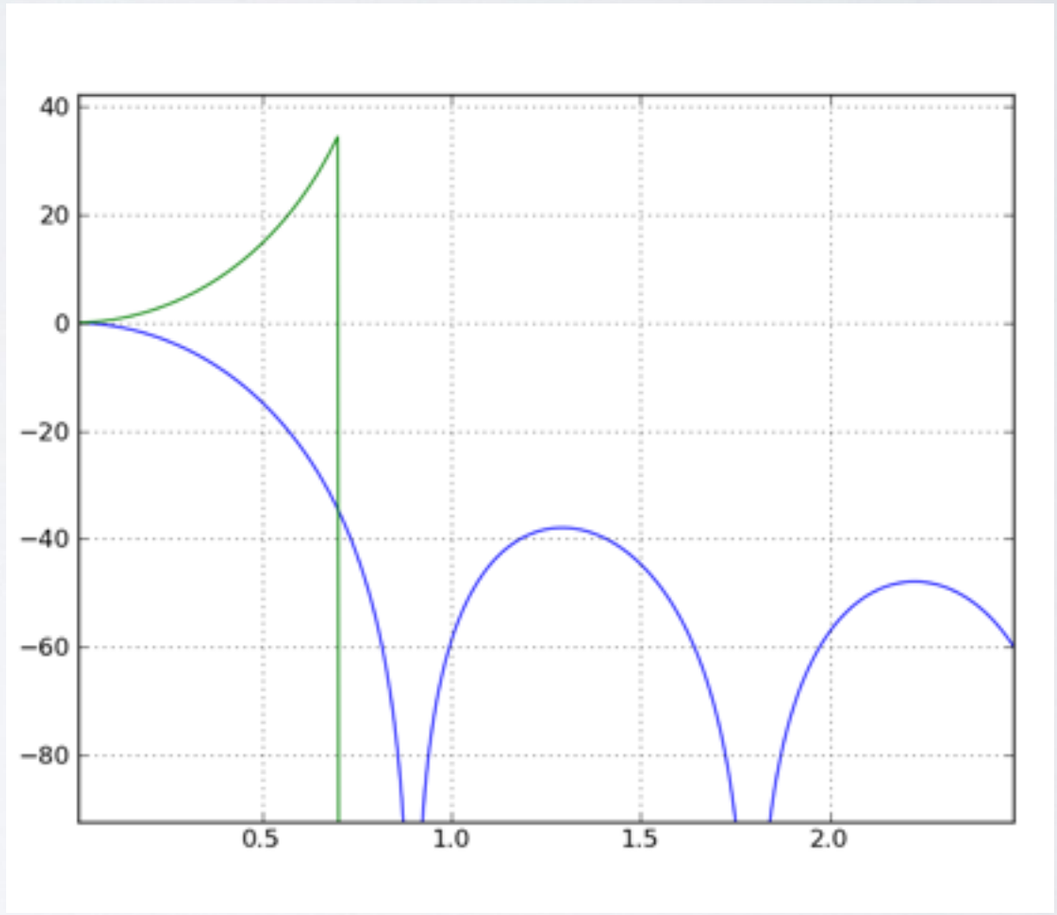
WHY CIC?

- "Cascaded Integrate and Comb" Filter
- Single pole decimator
- Uses only addition and subtraction
- Transition band is wide and not very flat



COMPENSATING FIR

- Compensates for CIC shape
- Narrow transition band
- Low decimation factor
- Uses one multiply per tap

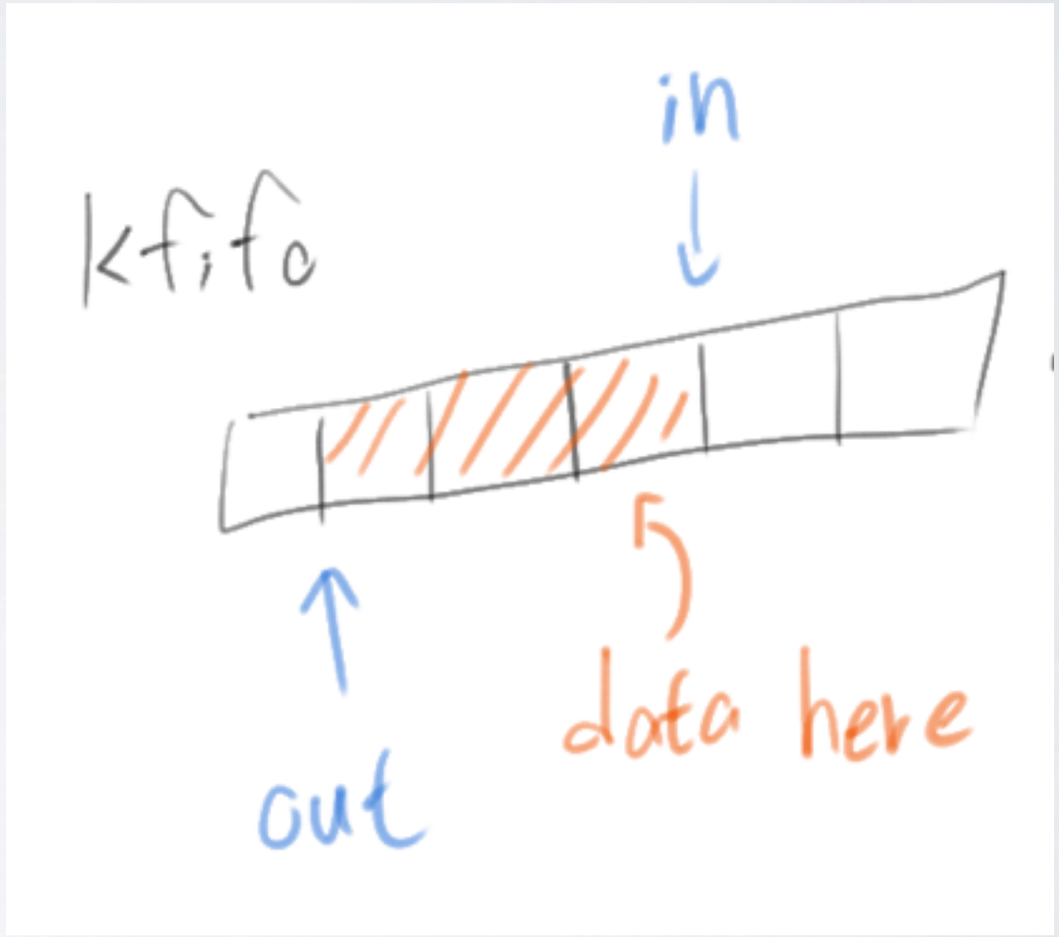


KERNEL DRIVER

- Hardware FIFO sends IRQ at configurable level

- Interrupt controller reads from Hardware FIFO into kernel FIFO

- read(2) reads out of the kernel FIFO



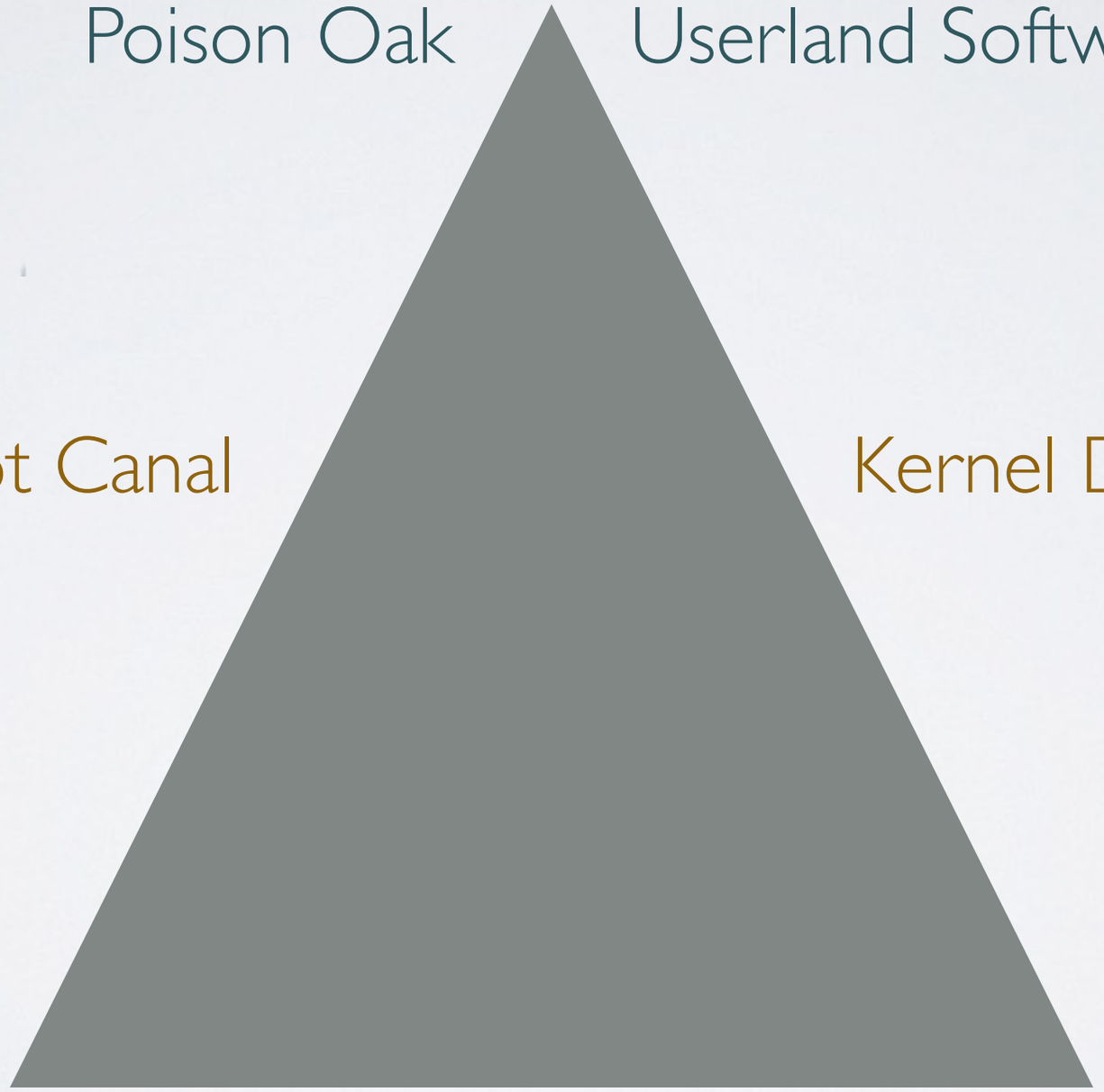
USERLAND DAEMON

- Reads from /dev/hpsdrrx0
- Manipulates controls in /sys
- Deals with all network traffic
- Multithreaded

HIERARCHY OF PAIN AND SUFFERING

Poison Oak

Userland Software



Root Canal

Kernel Driver

Amputation
Without Anesthetic

FPGA Firmware

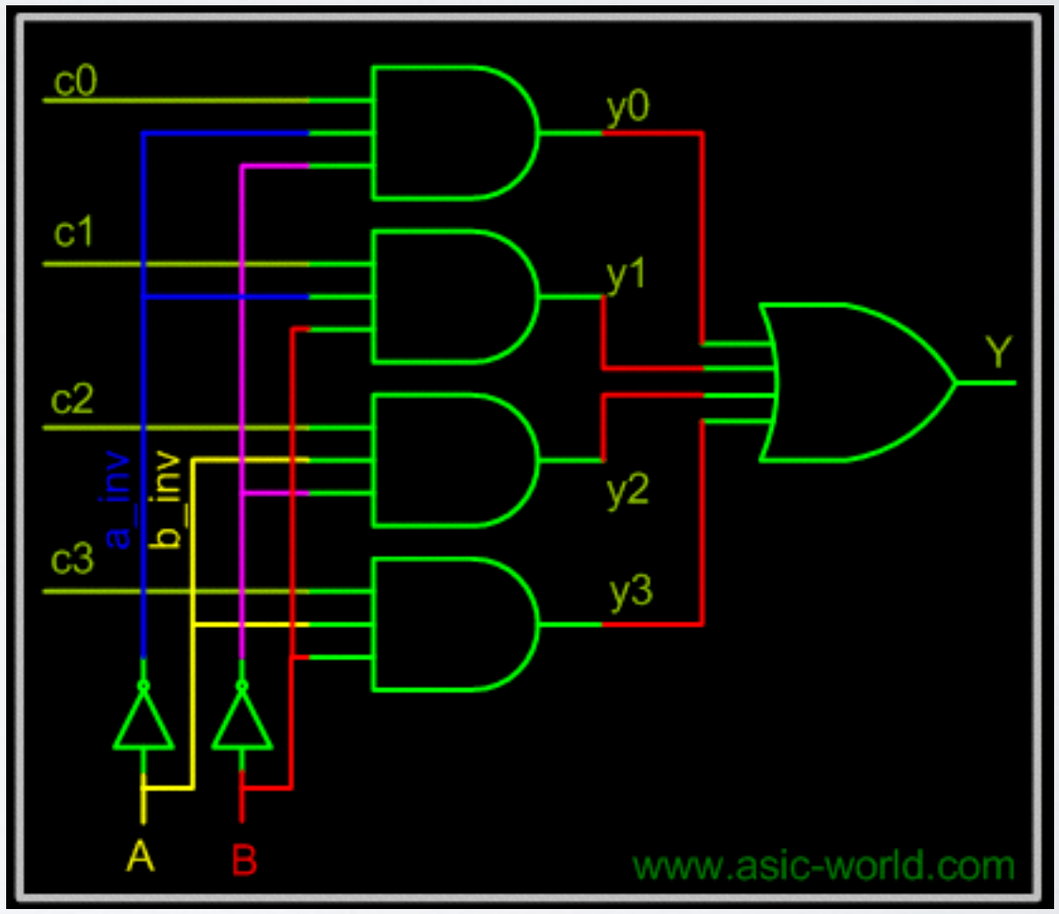
DEBUGGING TOOLS

- Userland: GDB, printf, etc.
- Kernel: KDB, kprintf, etc.
- FPGA: LEDs, SignalTap

```
1       ../sysdeps/i386/elf/start.S: No such file or directory.
        in ../sysdeps/i386/elf/start.S
gdb$ b main
Breakpoint 1 at 0x80483aa
gdb$ run
-------------------------------------------------------------------------[regs]
  EAX: BFFFF5FC  EBX: B7FCAFFC  ECX: B7FCD19C  EDX: 00000001  o d I t S z a P c
  ESI: BFFFF5F4  EDI: BFFFF580  EBP: BFFFF568  ESP: BFFFF550  EIP: 080483AA
  CS: 0073  DS: 007B  ES: 007B  FS: 0000  GS: 0033  SS: 007B
[007B:BFFFF550]-----------------------------------------------------------[stack]
BFFFF5A0 : 00 00 00 00  F8 0F 00 B8 - 01 00 00 00  D0 82 04 08 ................
BFFFF590 : 70 F5 FF BF  D2 4D EB B7 - 00 00 00 00  00 00 00 00 p....M..........
BFFFF580 : FC AF FC B7  00 00 00 00 - 80 F5 FF BF  C8 F5 FF BF ................
BFFFF570 : 01 00 00 00  F4 F5 FF BF - FC F5 FF BF  6C 5B FF B7 ............l[..
BFFFF560 : 00 00 00 00  E0 0C 00 B8 - C8 F5 FF BF  14 4E EB B7 .............N..
BFFFF550 : FC AF FC B7  FC AF FC B7 - 18 95 04 08  FC AF FC B7 ................
[007B:BFFFF550]-----------------------------------------------------------[data]
BFFFF550 : FC AF FC B7  FC AF FC B7 - 18 95 04 08  FC AF FC B7 ................
BFFFF560 : 00 00 00 00  E0 0C 00 B8 - C8 F5 FF BF  14 4E EB B7 .............N..
BFFFF570 : 01 00 00 00  F4 F5 FF BF - FC F5 FF BF  6C 5B FF B7 ............l[..
BFFFF580 : FC AF FC B7  00 00 00 00 - 80 F5 FF BF  C8 F5 FF BF ................
BFFFF590 : 70 F5 FF BF  D2 4D EB B7 - 00 00 00 00  00 00 00 00 p....M..........
BFFFF5A0 : 00 00 00 00  F8 0F 00 B8 - 01 00 00 00  D0 82 04 08 ................
BFFFF5B0 : 00 00 00 00  A0 5A FF B7 - B0 66 FF B7  F8 0F 00 B8 .....Z...f......
BFFFF5C0 : 01 00 00 00  D0 82 04 08 - 00 00 00 00  F1 82 04 08 ................
[0073:080483AA]-----------------------------------------------------------[code]
0x80483aa <main+6>:     and    esp,0xfffffff0
0x80483ad <main+9>:     mov    eax,0x0
0x80483b2 <main+14>:    add    eax,0xf
0x80483b5 <main+17>:    add    eax,0xf
0x80483b8 <main+20>:    shr    eax,0x4
0x80483bb <main+23>:    shl    eax,0x4
0x80483be <main+26>:    sub    esp,eax
0x80483c0 <main+28>:    mov    eax,ds:0x80484f4
0x80483c5 <main+33>:    mov    DWORD PTR [ebp-24],eax
0x80483c8 <main+36>:    mov    al,ds:0x80484f8
0x80483cd <main+41>:    mov    BYTE PTR [ebp-20],al
0x80483d0 <main+44>:    sub    esp,0xc
0x80483d3 <main+47>:    push   0x80484f9
0x80483d8 <main+52>:    call   0x80482b8 <printf@plt>
0x80483dd <main+57>:    add    esp,0x10
0x80483e0 <main+60>:    leave
-------------------------------------------------------------------------------

Breakpoint 1, 0x080483aa in main ()
gdb$
```

VERILOG

- Vendors only implement what they want
- Have to remember you're creating hardware
- Not all language constructs can be in hardware
- Testbench vs. Implementation



BUILD TIME

Userland

```
republic:openhpsdrd mcdermj$ time make

real    0m0.132s
user    0m0.088s
sys     0m0.034s
```

Kernel Module

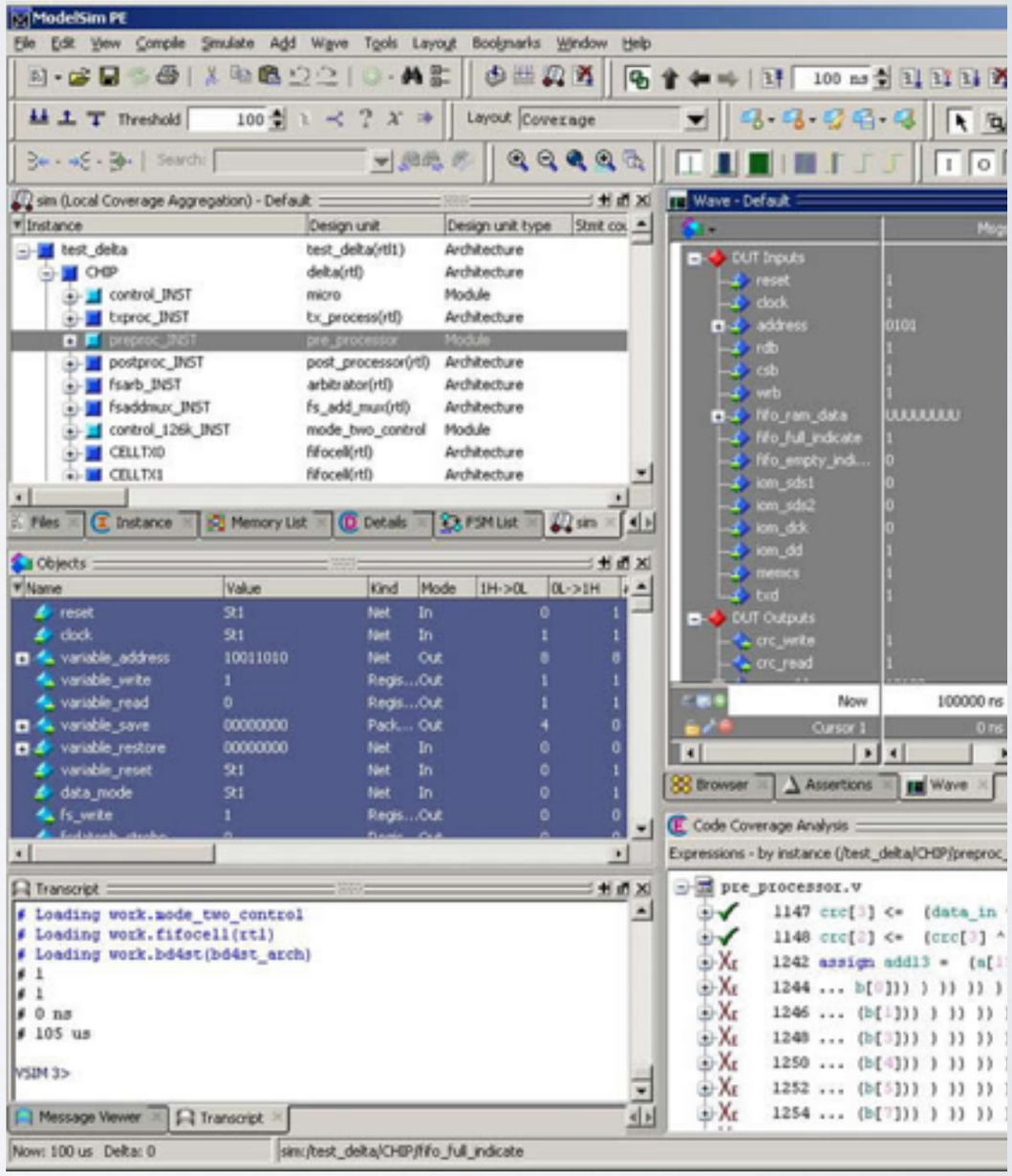
```
republic:hpsdr mcdermj$ time make default

real    0m1.046s
user    0m0.662s
sys     0m0.301s
```

FPGA

```
mcdermj@commune:~/sdrstick$ time make
real    12m8.360s
user    14m27.640s
sys     0m31.328s
```

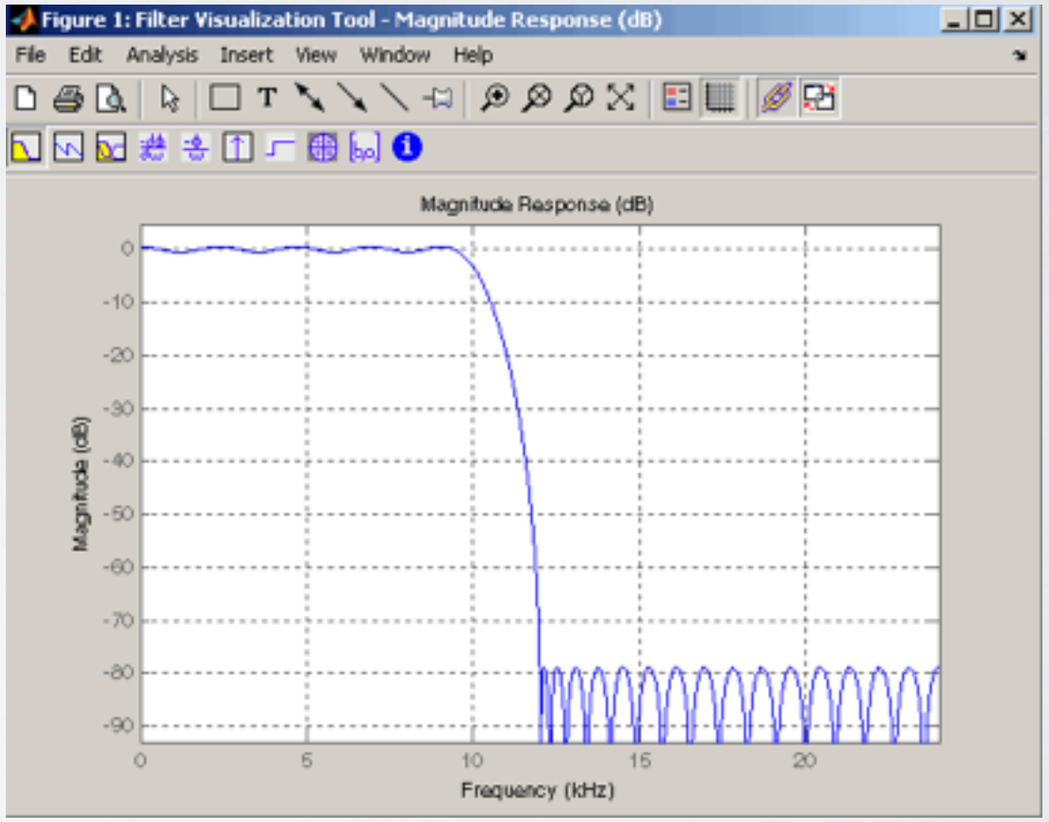
MODELSIM

- Useful for checking syntax before your 12 minute compile
- Unfortunately supports more of the standard than Quartus
- Just debugger enough to be annoying



MATLAB

- Great for filter design
- Yet Another Language
- Seems to not tell the whole story sometimes



QUESTIONS?

Software Developer

FPGA Developers
(In Natural Habitat)